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Effect of TMAH Etching Duration on the Formation of Silicon Nanowire Transistor Patterned by AFM Nanolithography

(Kesan Tempoh Punaran TMAH ke atas Penghasilan Transistor Nanodawai Silikon Tercorak Menggunakan Nanolitografi Mikroskop Daya Atom)

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ABSTRACT

Atomic force microscopy (AFM) lithography was applied to produce nanoscale pattern for silicon nanowire transistor fabrication. This technique takes advantage of imaging facility of AFM and the ability of probe movement controlling over the sample surface to create nanopatterns. A conductive AFM tip was used to grow the silicon oxide nanopatterns on silicon on insulator (SOI) wafer. The applied tip-sample voltage and writing speed were well controlled in order to form pre-designed silicon oxide nanowire transistor structures. The effect of tetra methyl ammonium hydroxide (TMAH) etching duration on the oxide covered silicon nanowire transistor structure has been investigated. A completed silicon nanowire transistor was obtained by removing the oxide layer via hydrofluoric acid etching process. The fabricated silicon nanowire transistor consists of a silicon nanowire that acts as a channel with source and drain pads. A lateral gate pad with a nanowire head was fabricated very close to the channel in the formation of transistor structures.

Keywords: Etching duration; nanolotography AFM; silicon nanowire; TMAH; transistor

ABSTRAK

Litografi mikroskop daya atom (AFM) telah diguna untuk menghasilkan corak skala nano untuk fabrikasi transistor nanowayar silikon. Teknik ini menggunakan kemudahan pengimejan AFM dan keupayaan mengawal pergerakan kuar di atas permukaan sampel untuk mewujudkan nanocorak. Hujung AFM yang konduktif telah digunakan untuk menghasilkan wafer nanocorak oksida silikon pada silikon di atas penebat (SOI). Voltan pada hujung sampel yang dikenakan dan kelajuan tulisan dikawal dengan baik untuk menghasilkan strukutur pra-bentuk transistor nanowayar silikon oksida. Kesan tempoh punaran tetra metil ammonium hidroksida (TMAH) terhadap oksida yang dilindungi struktur transistor nanowayar silikon telah dikaji. Transistor nanowayar silikon telah diperoleh dengan mengeluarkan lapisan oksida melalui proses punaran asid hidrofluorik. Transistor nanowayar silikon terdiri daripada nanowayar silikon yang bertindak sebagai saluran dengan pad sumber dan salir. Pad get sisi dengan kepala nanowayar telah direka bentuk berhampiran dengan saluran dalam pembentukan struktur transistor.

Kata kunci: Nanowayar silikon; nanolitografi AFM; tempoh punaran; TMAH; transistor

INTRODUCTION

Atomic force microscope (AFM) is a precision technique for surface topography analysis. AFM lithography has recently attracted much interest for the fabrication of nanoscale devices which is an easy method for achieving nanometer resolution. Moreover, the AFM can be used to investigate not just conducting material but also for insulating material like polymer (Xie et al. 2006). There are several types of nanostructures such as GaAs oxide, silicon oxide and metal thin film which can be produced by AFM nanolithography via local anodic oxidation (LAO) process (Fu et al. 1999; Giesbers et al. 2008; Held et al. 1998; Hu & Hu 2005; Lazzarino et al. 2006; Lee et al. 2004). In a LAO patterning method, the oxide will grow on a chemically reactive substrate by the application of a voltage between a conductive AFM tip and a substrate surface. There is a threshold voltage at which the anodic oxidation can be started. The water molecules adsorbed on a substrate dissociates into fragments (e.g. H^+, OH^- and O^{2-}) due to high electric field ($E > 10^7$ V/m) between tip and substrate. This ionized water will be acted as an electrolyte to form oxide pattern (Cervenka et al. 2006). There are some parameters that will influence the LAO patterning such as tip voltage, tip writing speed, humidity and oxidation time. These parameters have been proven to influence the patterning process (Cervenka et al. 2006; Fang 2004; Fu et al. 1999; Held et al. 1998; Hu & Hu 2005; Hutagalung et al. 2007; Kuramochi et al. 2003; Luo et al. 2006).

The silicon nanowire transistor (SiNWT) can be produced by wet chemical etching process of the AFM nanolithography patterned device structures (Lew & Hutagalung 2010). For wet chemical etching process, the selection of etchant solution is very important in order to produce a good formation of device structure. In this

work, the tetramethylammonium hydroxide (TMAH) and hydrogen fluoride (HF) acid have been used. HF acid is an isotropic chemical etchant and it is used to remove the oxide layer. Meanwhile, an anisotropic chemical etchant of TMAH is used for silicon layer removal. The TMAH etchant has been choose due to its high ratio of etching selectivity to silicon, non-flammable, non-toxic, less harmful and CMOS compatible (Chien et al. 2002; Choi et al. 1998; Xuefeng 2005).

SiNWT has become very interactive and has potential to build up the nanoelectronics industry. Nanowires are one dimensional nanostructure with good electrical properties; making them suitable for the nano-scale devices fabrication (Lee et al. 2009). Silicon nanowire transistor can be fabricated by top-down approach and bottom-up approach which depends on the application (Yoon et al. 2008). For the potential application in the integrated circuits, the bottom-up approach provides cost-effective nanowires fabrication if compared with the top-down approach (Yoon et al. 2008). There are many techniques developed for silicon nanowires transistor fabrication such as chemical-vapour-deposition (CVD), electron-beam lithography, laser induced decomposition, and field-emission induced growth on a scanning tunneling microscopy tip (Lee et al. 2009; Salem et al. 2009; Suk et al. 2008; Yoon et al. 2008). To date, the research on fabrication of SiNWT via AFM nanolithography are very limited.

Therefore, in this paper, the SiNWT was designed by AFM lithography patterning via LAO mechanism and followed by two steps of wet chemical etching processes. The size and morphology of the fabricated SiNWT were analyzed by AFM and variable pressure field emission scanning electron microscope (VPFESEM).

EXPERIMENTAL METHOD

The silicon nanowire transistor (SiNWT) was fabricated on the surface of the p-type silicon-on-insulator (SOI) wafer (SOITEC, 100 nm Si layer, 14-22 Ωcm, and 200 nm SiO_2 buried oxide) by AFM nanolithography method. The local anodic oxidation process was performed by using a scanning probe microscope (SPM) machine (SPI3800N/4000) with conductive AFM mode operated in contact mode. A conductive AFM tip (overall gold coating tip) was used to draw pre-designed nanoscale oxide pattern of transistor structure. The oxide pattern acted as a mask for the wet chemical etching process to produce the SiNWT. Prior to use, the SOI wafer was cut into small size (1 cm × 1 cm), cleaned by standard cleaning process and then passivity by hydrogen fluoride (HF) acid to avoid contaminant and native oxide. The nanoscale oxide pattern was drawn on the pre-cleaned surface of SOI wafer with applied tip voltage of 7, 8 and 9 V at tip writing speed of 6 μm/s and 9 μm/s at humidity 55.8%RH - 68.9%RH. In order to produce a SiNWT, the patterned sample was wet chemical etched in 25 wt% tetramethylammonium hydroxide (TMAH) in water solution at 65°C for different etching time from 10 to 35 s. The objective of this etching stage was to remove the uncovered silicon layer by nanoscale oxide pattern and remain the oxide capped SiNWT. The SiNWT obtained by removing the oxide layer using 2 wt% hydrogen fluoride (HF) acid. Schematic diagram of SiNWT fabrication by AFM lithography is shown in Figure 1. The size and surface topography of fabricated device structures were observed using AFM topography mode during the patterning process as well as after wet chemical etching process. In addition to AFM observation, the FESEM analysis was performed to the fabricated device to study its microstructures.

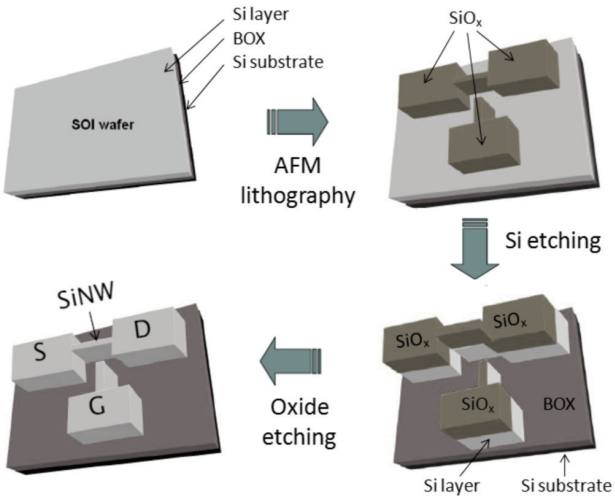

FIGURE 1. Schematic diagram of SiNWT fabrication by AFM lithography followed by wet chemical etching processes. The SiOx mask is patterned on SOI wafer via local anodic oxidation by AFM lithography, uncovered Si layer etched by TMAH, SiNWT obtained after removing oxide mask

RESULTS AND DISCUSSION

The SiNWT structure with components of a source (S), a drain (D), a gate (G) and a silicon nanowire as channel was patterned as a nanoscale oxide layer structure on the SOI wafer surface. Figure 2 shows the two and three dimensional AFM images of the SiNWT structures patterned by applied tip voltage of 7, 8 and 9 V with tip writing speed of 6 μm/s and 9 μm/s, respectively. The topography contour scale value in the AFM images increased when the applied tip voltage was increased. This can conclude that the thickness of the pre-designed nanoscale oxide pattern of the SiNWT structure increased due to the increment of the applied tip voltages.

Quantitative analysis of effect of applied tip voltage and tip writing speed on the formation of oxide pattern of SiNWT structures are shown in Figure 3. From the measurement, the thickness of the oxide pattern is increasing linearly with the applied tip voltage. The oxide pattern thickness increased from 1.25 nm for 7 V applied voltage to 2.35 nm for 8 V at a constant tip writing speed of 9 μm/s. For 9 V tip voltage, the thickness of the oxide pattern was about 4.50 nm. These phenomena are similar to the previous reported

works that the width and thickness of the AFM patterned silicon oxide lines, oxide nanodots and oxide protrusions are increased with the applied tip voltage (Cervenka et al. 2006; Fang 2004; Hutagalung et al. 2007).

At slower tip writing speed the of 6 μm/s, the thickness of the oxide pattern increased linearly from 1.50 to 5.50 nm when applied tip voltage increased from 7 to 9 V. Figure 3 also shows that the slower tip writing speed of 6 μm/s produced a higher oxide pattern thickness compared with 9 μm/s tip writing speed at the same applied tip voltage. The slower tip writing speed will produce thicker oxide pattern due to longer exposure time during patterning.

Based on the results in Figure 3, the tip writing speed of 6 μm/s and applied tip voltage of 9 V have been chosen as the most suitable parameters for the SiNWT patterning process by AFM lithography. The patterned SiNWT structure was etched with TMAH to remove uncovered silicon layer (100 nm thickness) up to the buried oxide layer that act as etched stop. The etching process was done at 65°C for different etching time from 10 to 35 s using 25 wt% TMAH in water solution. Figure 4 shows the 2D and 3D AFM images of the patterned SiNWT and TMAH etched structures. From the 2D AFM images in Figure 4, the topography contour scale value of the device after etched by TMAH is higher if compared with the contour scale of before etched oxide patterns. Typical contour scale of device before and after TMAH etched for 35 s are 7.91 nm and 168.95 nm, respectively. These results proved that uncovered silicon layer has been removed partially or completely by TMAH etching and formed the oxide covered SiNWT structure. From 3D AFM observation in Figure 4 it was found that TMAH etching on silicon layer are uniform and produced smooth surface. These results proved that the TMAH etchant provided good etching uniformity and high selectivity to silicon with respect to the oxide masking layer as reported by Dalla et al. (2008).

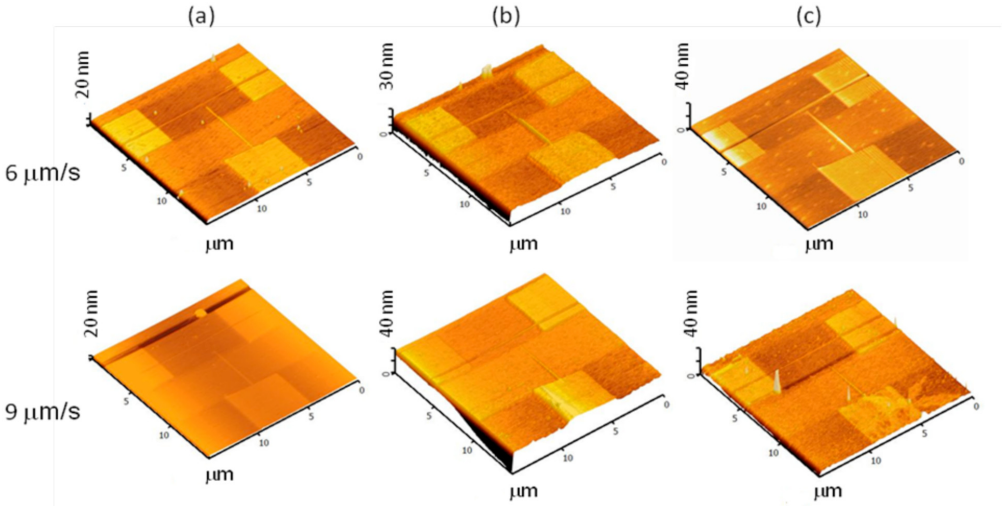

FIGURE 2. AFM images of the SiNWT structures patterned by applied tip voltage of (a) 7 V, (b) 8 V and (c) 9 V with tip writing speed of 6 μm/s and 9 μm/s, respectively

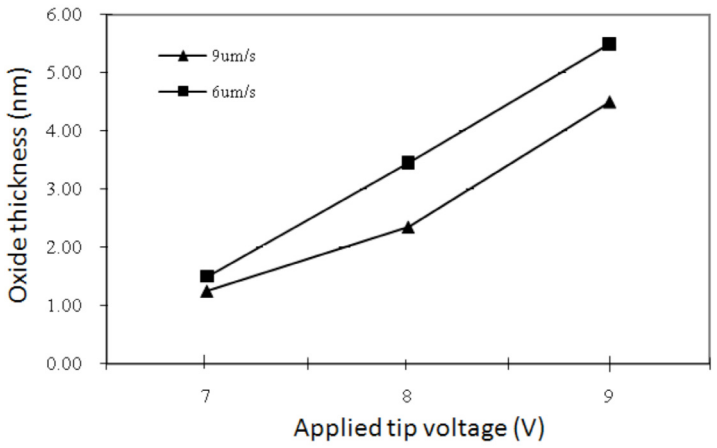

FIGURE 3. Graph of effect of applied tip voltage and tip writing speed on the oxide pattern thickness of SiNWT structure

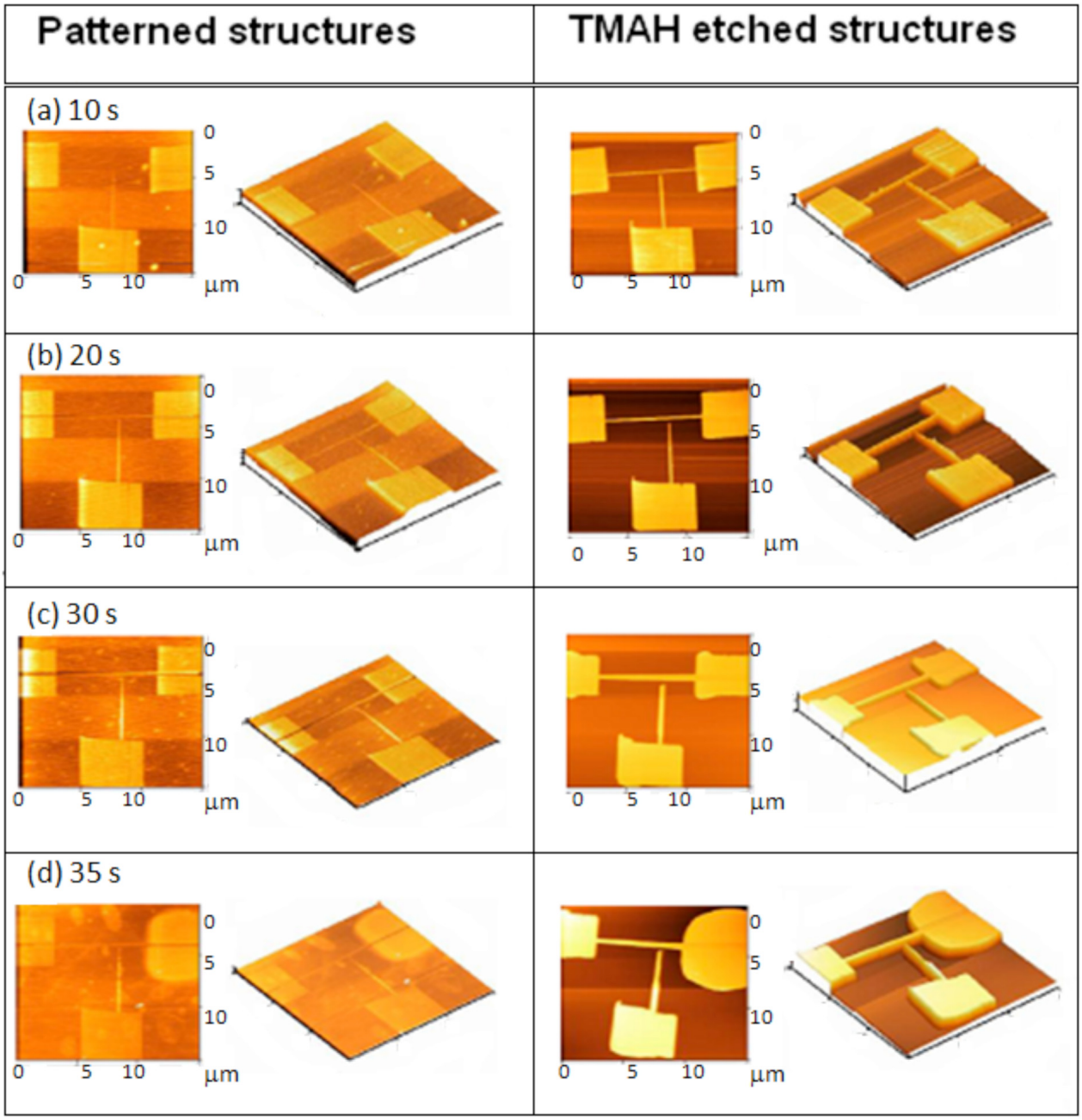

FIGURE 4. Selected 2D and 3D AFM images of SiNWT structures before and after etched with 25 wt% TMAH at 65°C for 10 - 35 s

Besides the surface topography observation, the thickness of removed silicon layer was estimated by comparing the measured thickness of the SiNWT structure before and after TMAH etching. Figure 5 shows the thickness of the removed silicon layer after etched with 25 wt% TMAH measured at source (S) pad, drain (D) pad, wire channel, gate (G) and gate (G) pad. It was found that the thickness of etched silicon layer increased with etching time. By prolong etching time, more silicon elements can be removed from SOI surface until at saturation condition at 35 s. As shown in Figure 5, measured thickness at the S pad, D pad, G pad and nanowire channel of the device are not much different for each etching time. For 10, 12, 15, 20, 25, 30 and 35 s etching time the removed thickness of silicon layer are 36.13 nm, 38.73 nm, 38.83 nm, 54.89 nm, 70.70 nm, 95.71 nm and 100.59 nm, respectively. The results indicated that TMAH etching for 30 s or longer was able to remove completely uncovered silicon layer from top of SOI wafer (Si layer thickness of SOI is 100 nm) to form oxide covered SiNWT structure.

Figure 6 shows the AFM and FESEM images of the SiNWT structures obtained after TMAH and HF etching processes. These images show that a completed SiNWT device has been fabricated by AFM nanolithography followed by wet chemical etching processes. Both of the images show very smooth surface morphology after etched

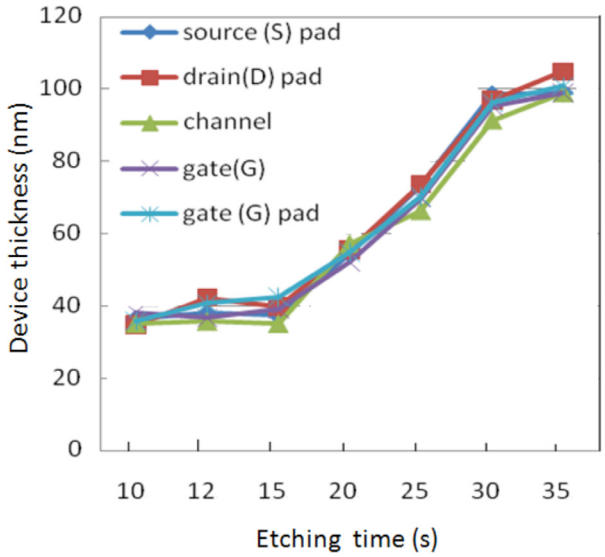

FIGURE 5. Effect of etching time on device thickness after etched with 25 wt% TMAH in water solution at 65°C for different etching time in the range of 10 - 35 s

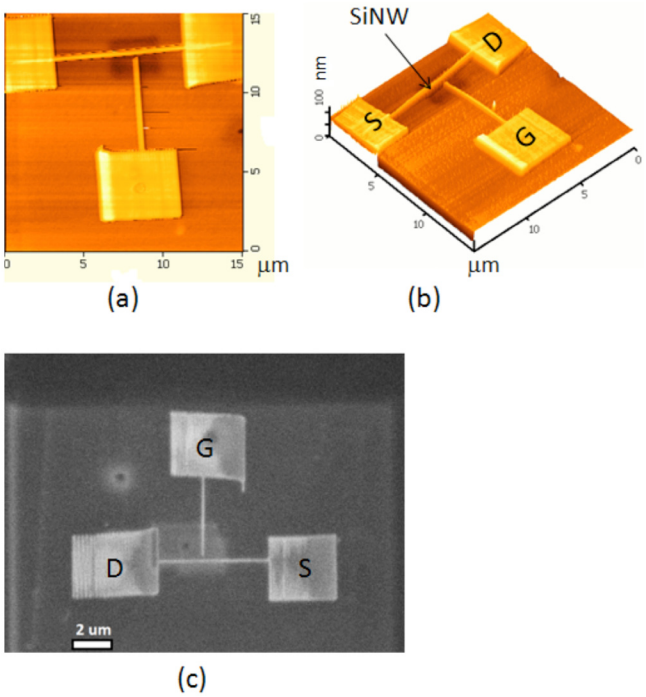

FIGURE 6. A completed SiNWT device obtained after TMAH and HF etching processes: (a) 2D and (b) 3D AFM images and (c) FESEM image

by TMAH and HF. Choi et al. (1998) reported that TMAH etchant is a reliable etchant agent to produce smooth and uniform silicon nanostructure. SiNWT device with about 90 nm width of the wire had been successfully fabricated.

CONCLUSION

As a conclusion, the silicon nanowire transistor (SiNWT) with components of a source (S), a drain (D), a gate (G) and a silicon nanowire as channel has been successfully fabricated by AFM nanolithography patterning followed by wet chemical etching processes. This can be achieved by well controlling the processing parameters such as applied tip voltage, tip writing speed and TMAH etching duration.

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